8 - Schematics hl9_15

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Note: Schematic Diagrams that were not amended are included in the hl9_14 diagrams

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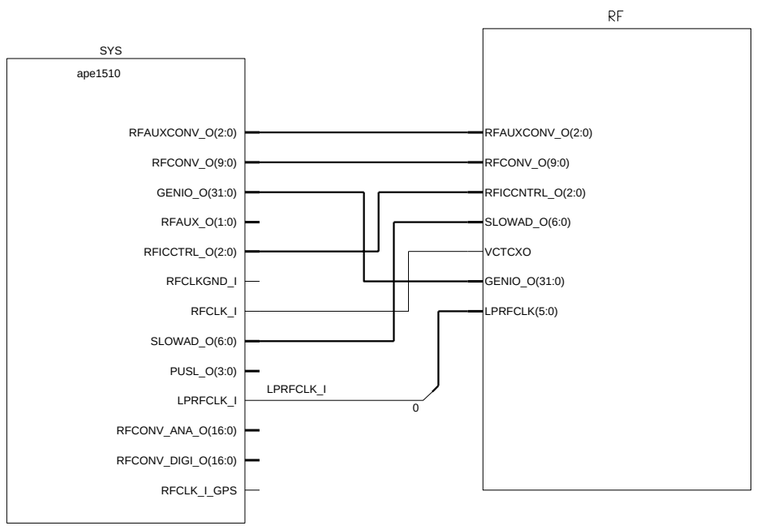
Main Level v.5.0, ed.117



Component References:			
SYS_CONN	2000 - 2099	APE_AUDIO	4100 - 4199
PRODUCTIONTESTPATTERN	2060 - 2069	APE_POWER	4200 - 4399
AUDIO	2100 - 2199	APE_UI	4400 - 4599
POWER	2200 - 2399	APE_CPU	4800 - 4899
KEY_UI	2400 - 2599	APE_MEMORY	5000 - 5099
SIM	2700 - 2799	APE_SDRAM	5080 - 5099
UPP	2800 - 2899	APE EMU	5100 - 5199
RF-BB	2900 - 2999	APE_MMC	5200 - 5299
MEMORY	3000 - 3099	APE_LPRF	6000 - 6099
EMU	3100 - 3199		
JTAG	3100 - 3179		
OSTRICH	3180 - 3189		
		RF	7000 - 7399
		TRANSMITTER	7000 - 7099
		RECEIVER	7100 - 7199
		SYNTHESIZER	7200 - 7299
		RF COMMON	7300 - 7399

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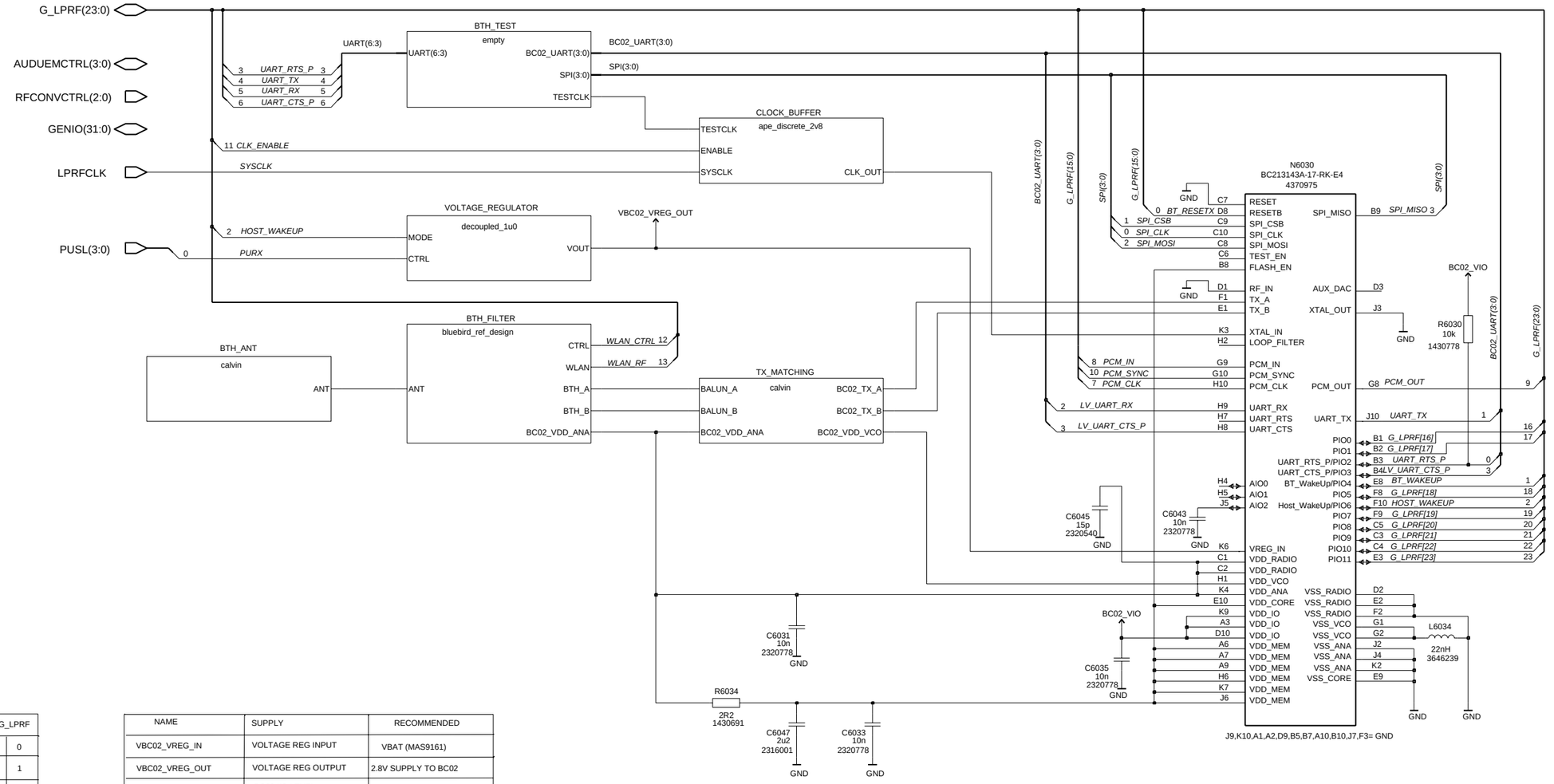
Bluetooth Circuit v.2.0, ed.73



NAME	G_LPRF
BT_RESETX	0
BT_WAKEUP	1
HOST_WAKEUP	2
UART_RTS_P	3
UART_TX	4
UART_RX	5
UART_CTS_P	6
PCM_CLK	7
PCM_IN	8
PCM_OUT	9
PCM_SYNC	10
CLK_ENABLE	11
WLAN_CTRL	12
WLAN_RF	13

NAME	SUPPLY	RECOMMENDED
VBC02_VREG_IN	VOLTAGE REG INPUT	VBAT (MAS9161)
VBC02_VREG_OUT	VOLTAGE REG OUTPUT	2.8V SUPPLY TO BC02
VBC02_VIO	BC02 I/O LEVEL	1.8V
VBC02_CLK_BUFF	CLOCK BUFFER	2.8V or 1.8V
VBC02_RF_SWITCH	WLAN RF SWITCH	2.8v (WLAN / APE)

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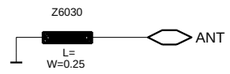
Bluetooth Antenna Connection v.1.0, ed.20



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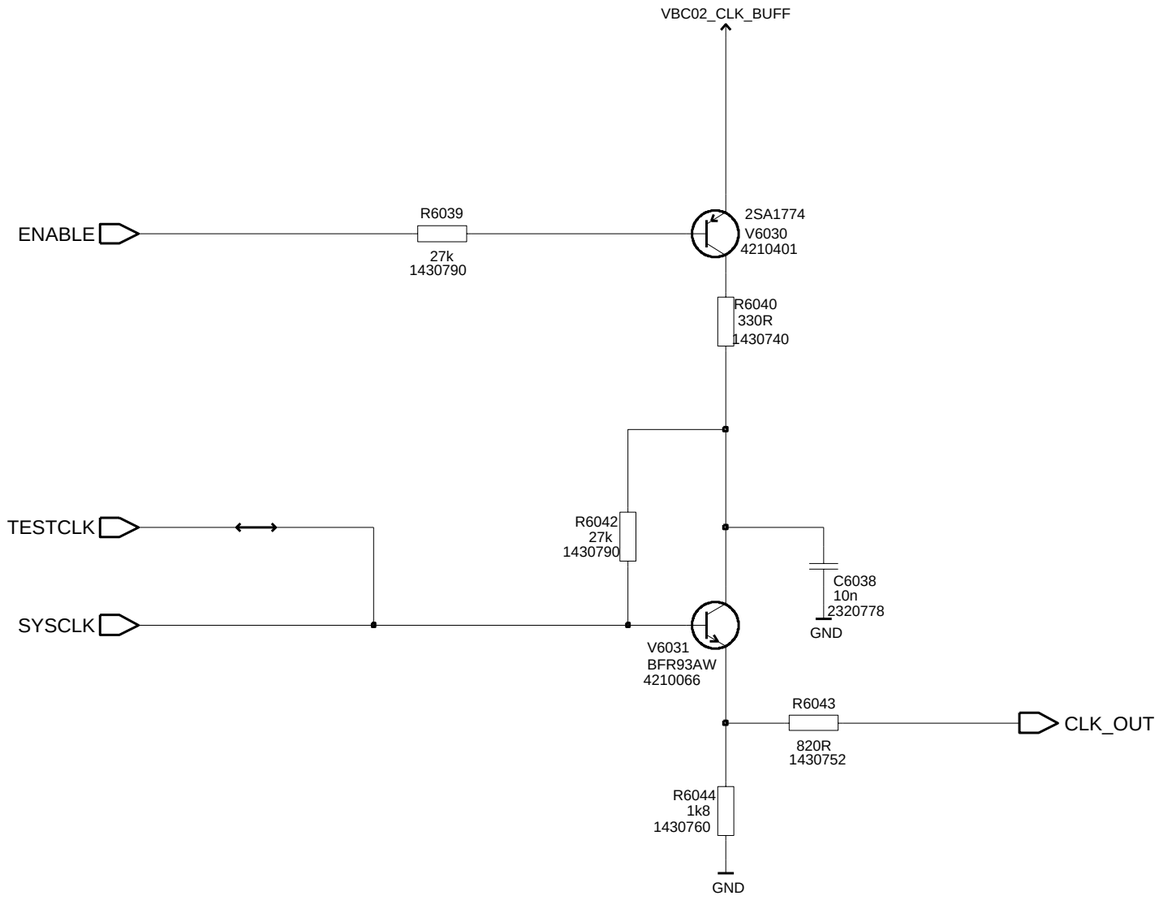
Clock Buffer for 12MHz Clock from APE v.1.0, ed.14

BLUETOOTH CLOCK BUFFER CIRCUIT

FOR 12MHZ CLOCK FROM APE1510

2.8V SUPPLY VOLTAGE



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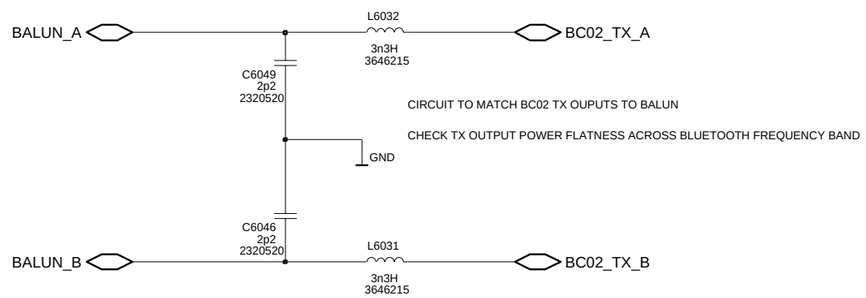
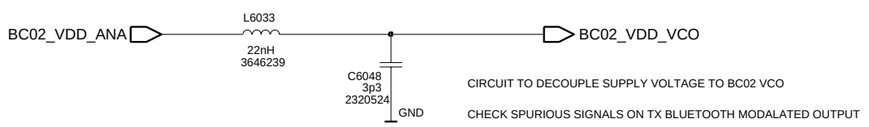
Tx Matching Circuit v.2.0, ed.21





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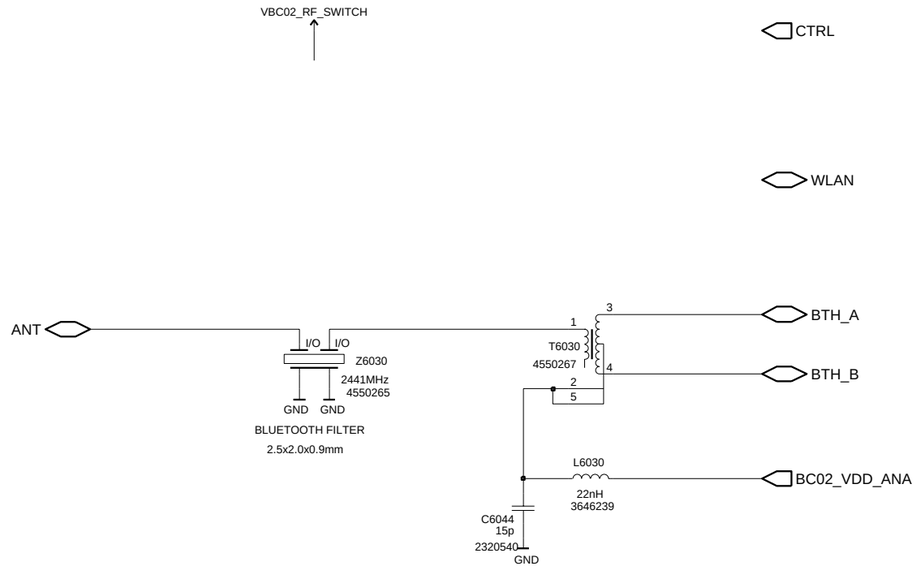
Bluetooth Filter and Balun v.1.0, ed.10



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Voltage Regulator v.14, ed.15

DECOUPLING CAPACITOR FOR 2V8 REGULATED SUPPLY

FROM APE1510

MODE

CTRL

VOUT

C6036
1u0
2320481

GND

!!! CAUTION: THIS SHEET OMITS THE EXTERNAL VOLTAGE REGULATOR

CHECK THAT THE REGULATED SUPPLY MEETS BC02 REQUIREMENTS BEFORE USING THIS SHEET.

ALSO CHECK THAT BLUETOOTH CIRCUIT DOES NOT DEGRADE SUPPLY VOLTAGE.

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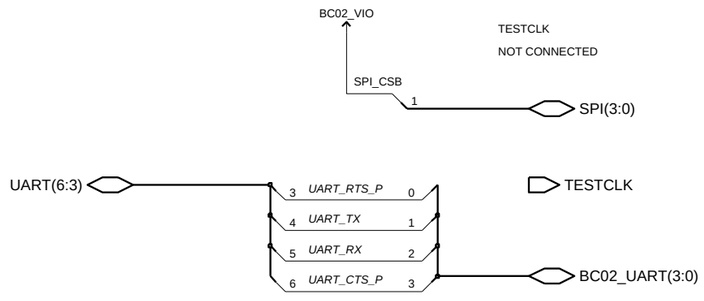
Bluetooth Test Interface v.1.0, ed.16

TEST INTERFACE COMPONENTS AND PADS REMOVED



UART LINES CONNECTED DIRECTLY TO BC02

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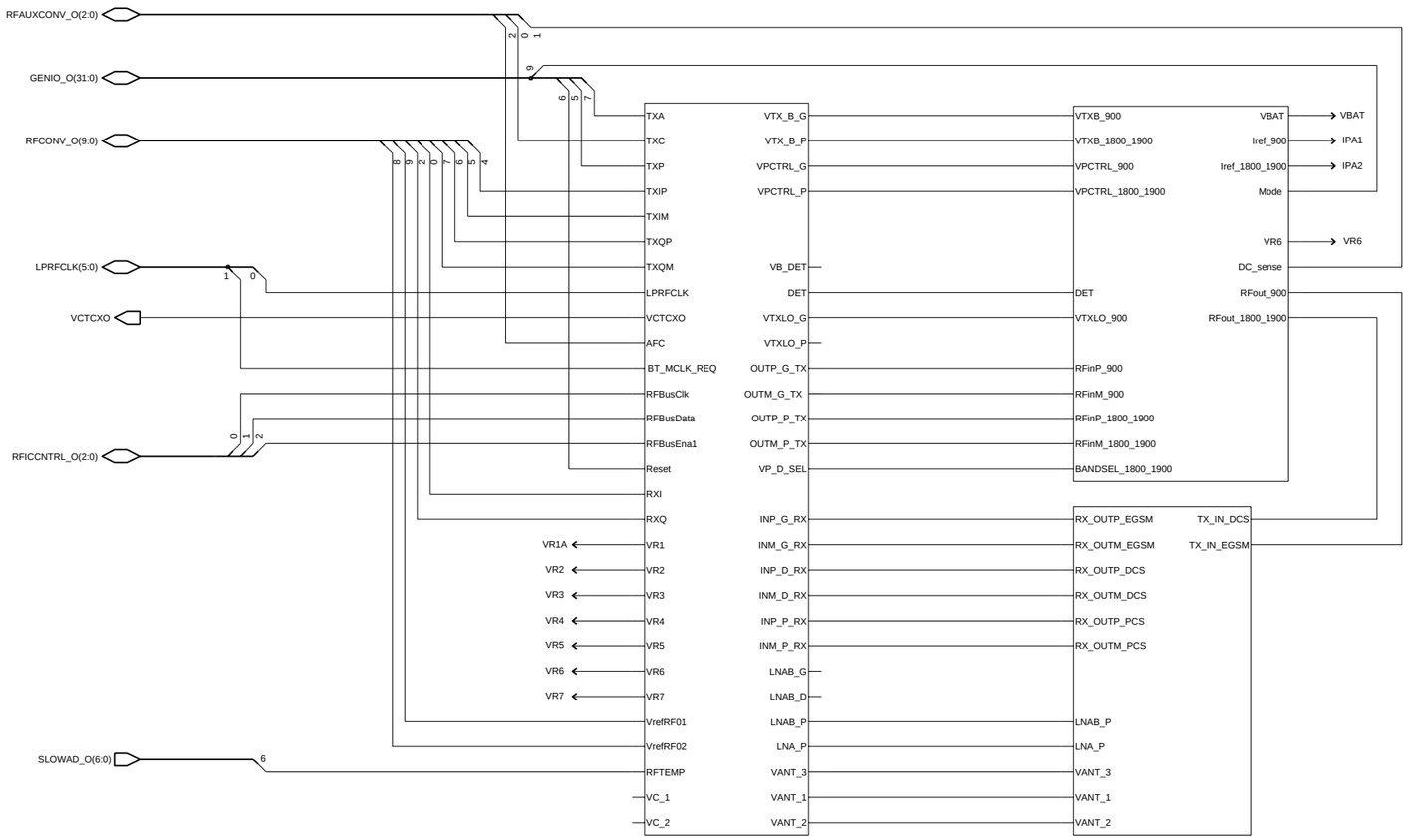
RF Top Level v.0.1, ed. 60



Last references:

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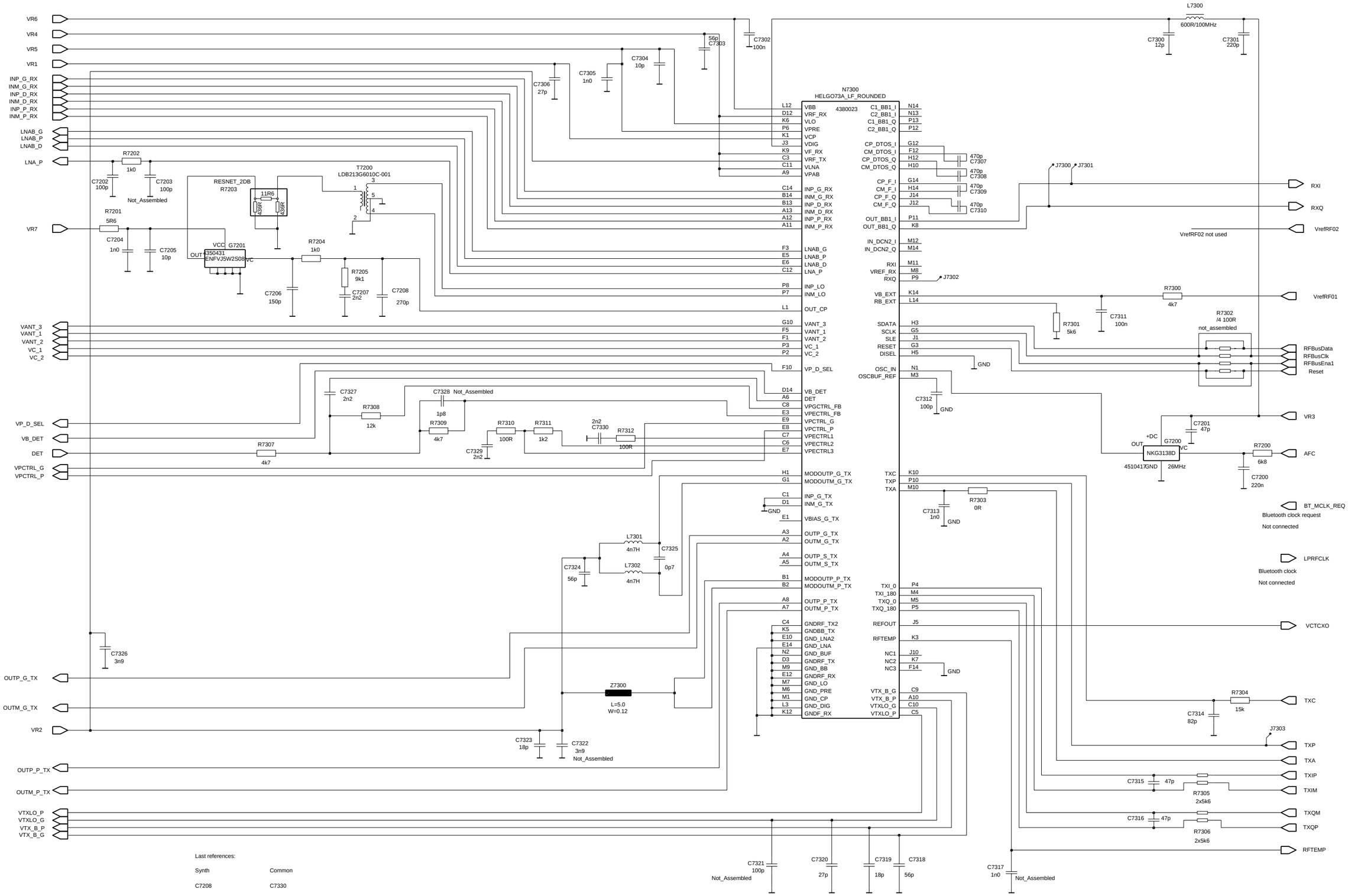
Helgo v.4.0, ed.117



Last references:

Synth	Common
C7208	C7330
G7201	J7303
R7205	L7302

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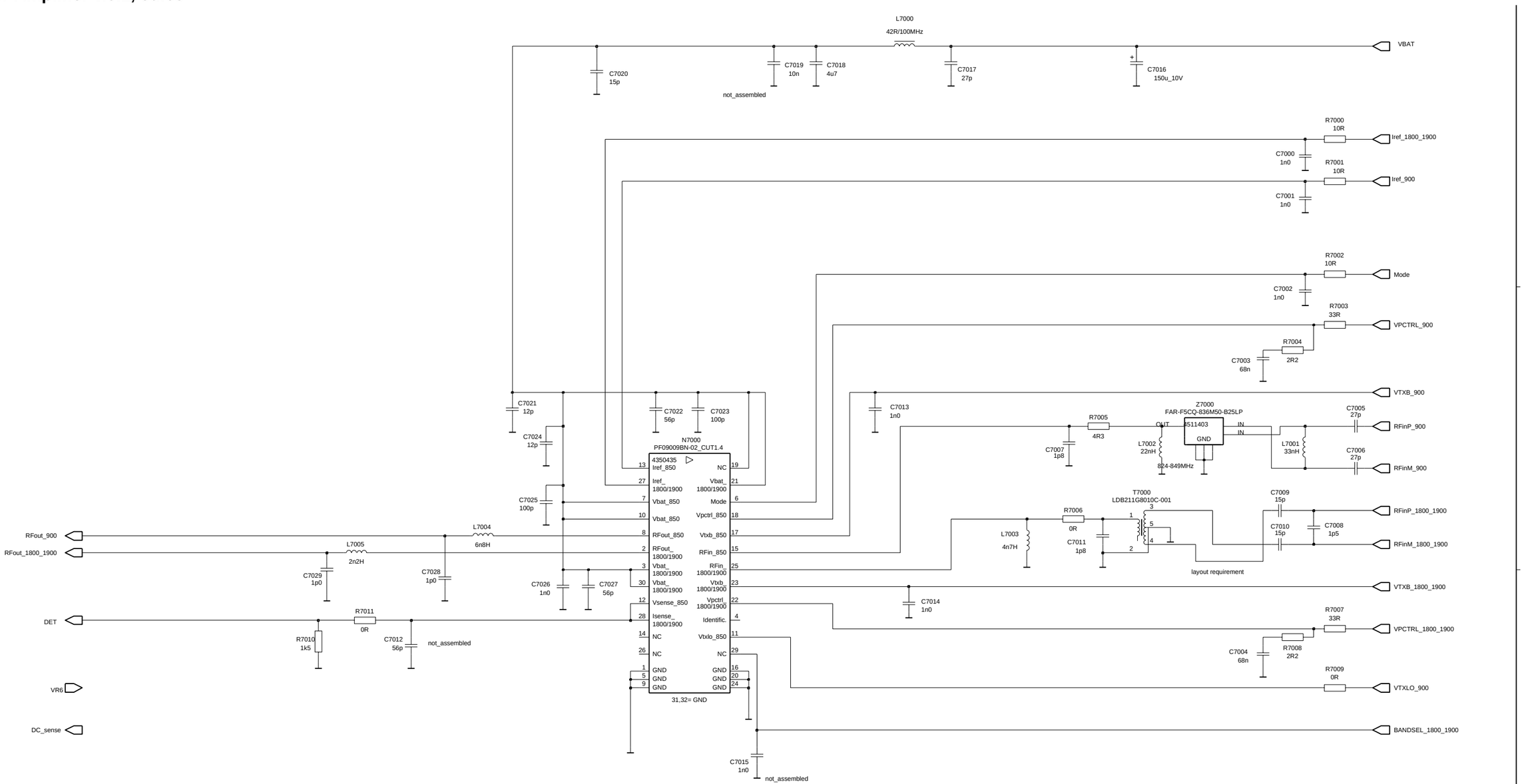
Power Amplifier v.0.1, ed.65



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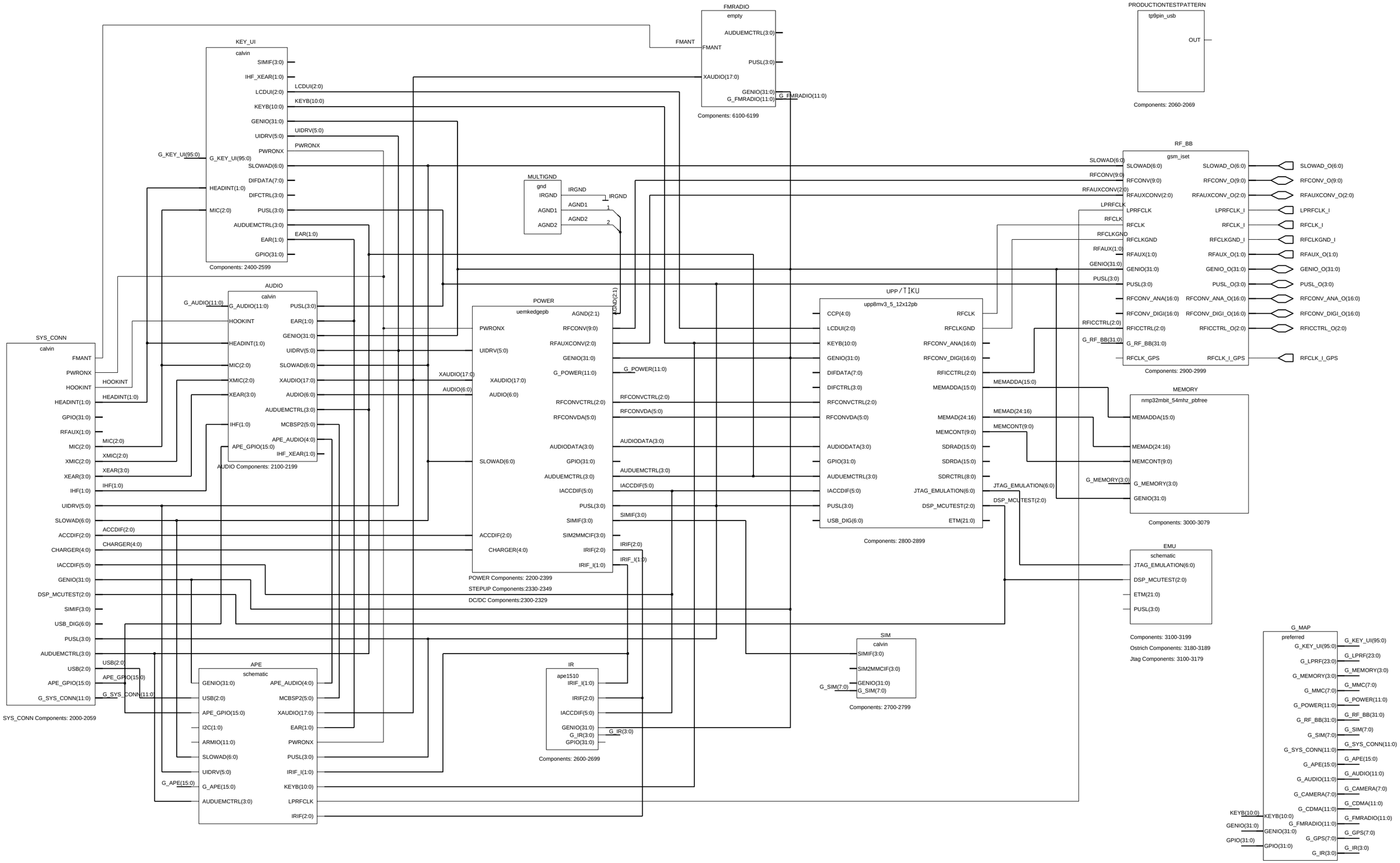
BB Top Level v.0.0, ed.42



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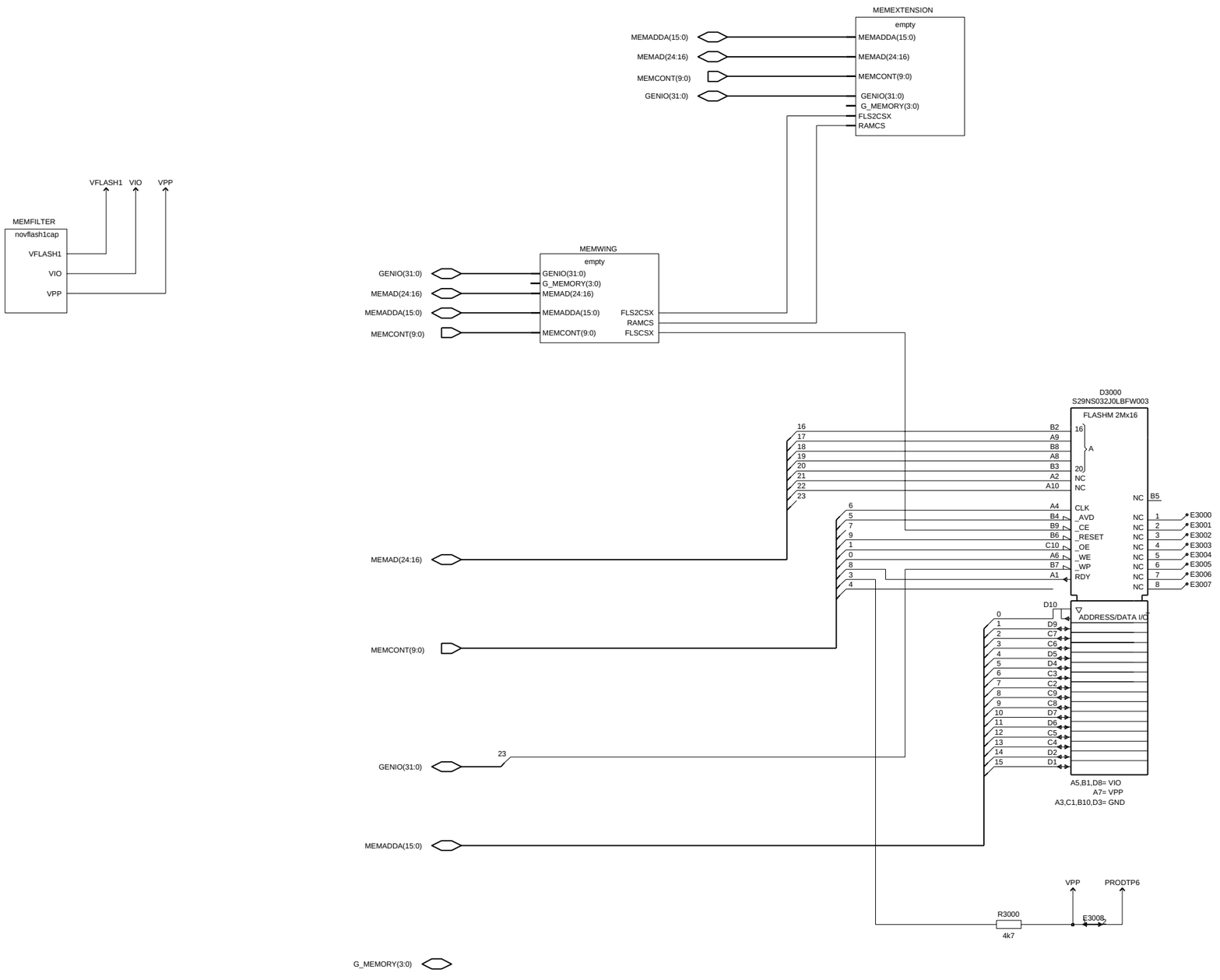
Flash Memory v.2.0, ed.44



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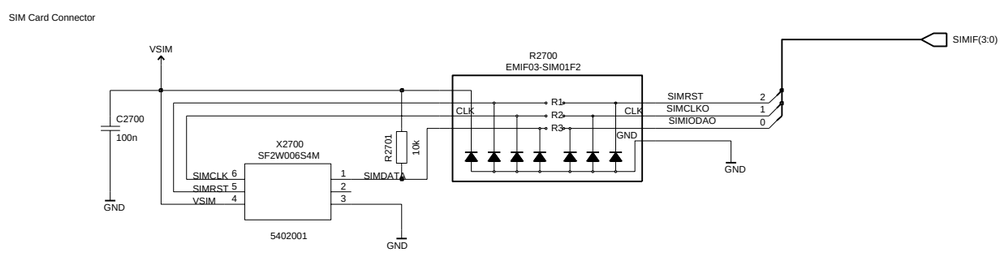
SIM Reader v.0.0, ed.12

SIM2MMCIF(3:0)

GENIO(31:0)

G_SIM(7:0)



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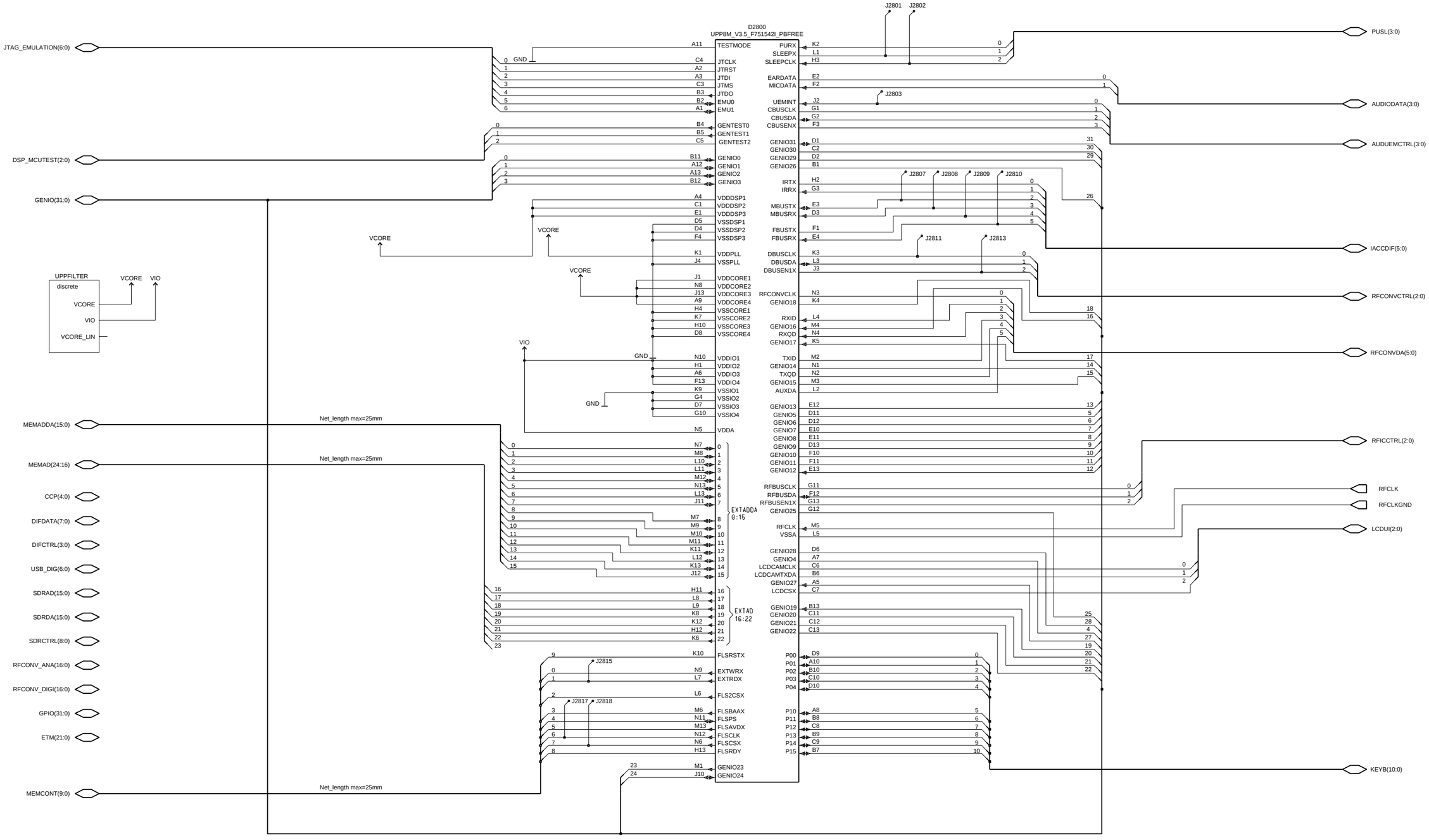
UPP8M v.2.0, ed.111



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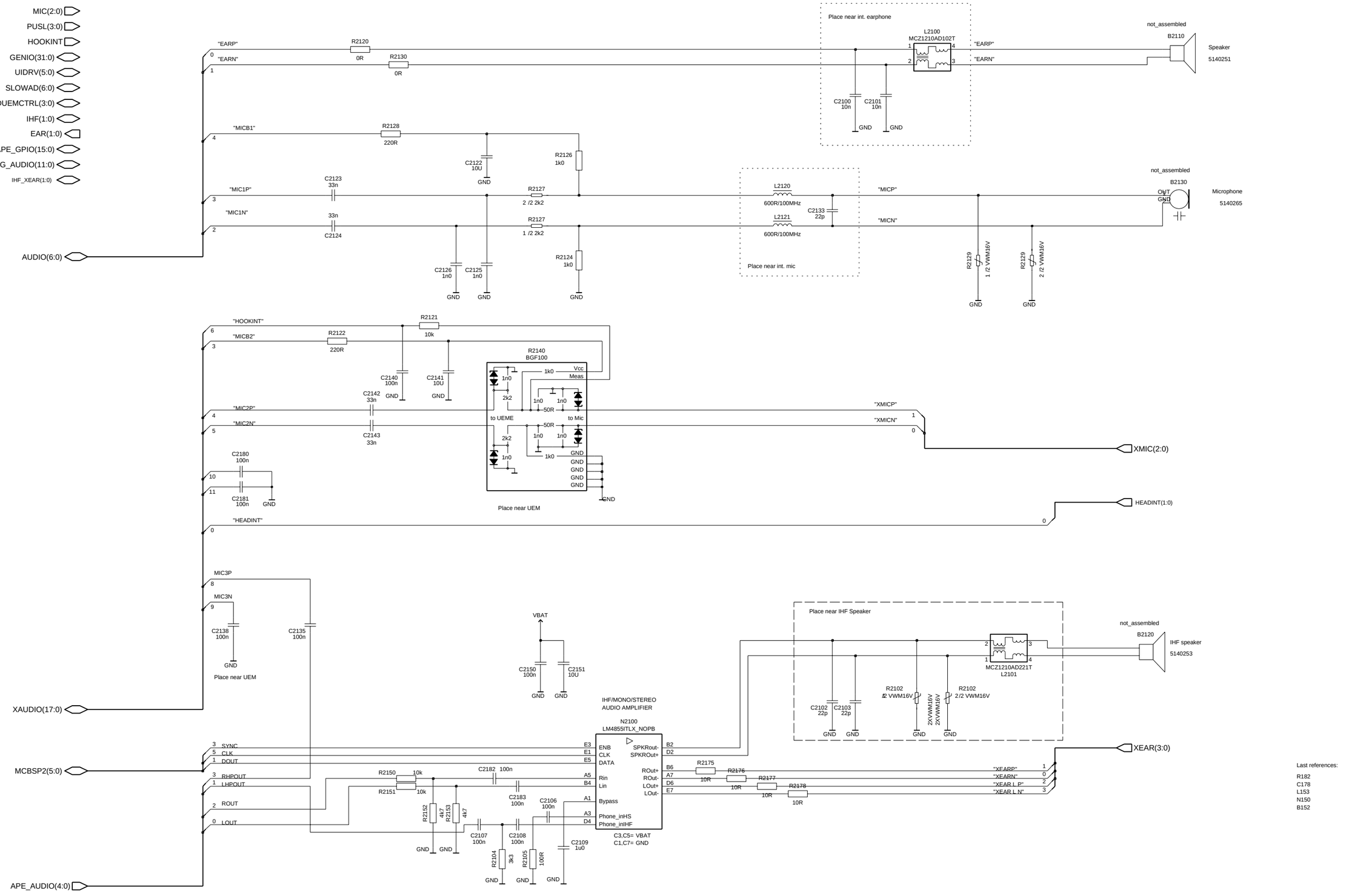
CMT Audio v.0.0, ed.48



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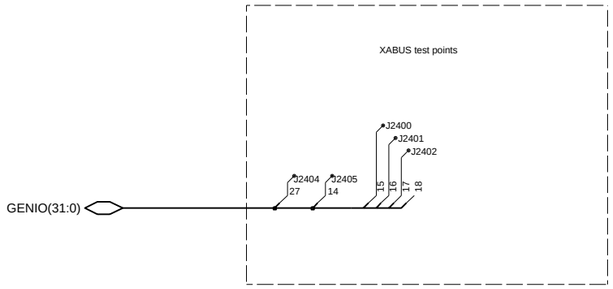
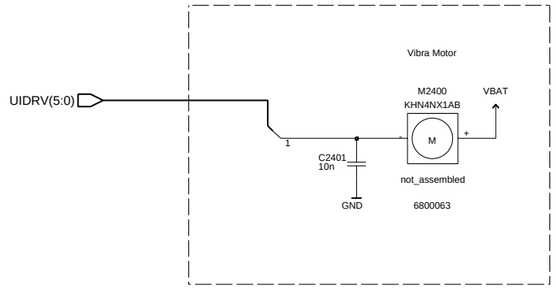
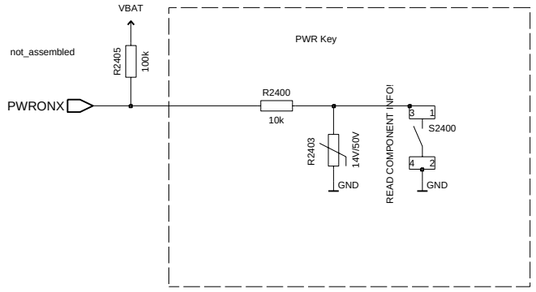
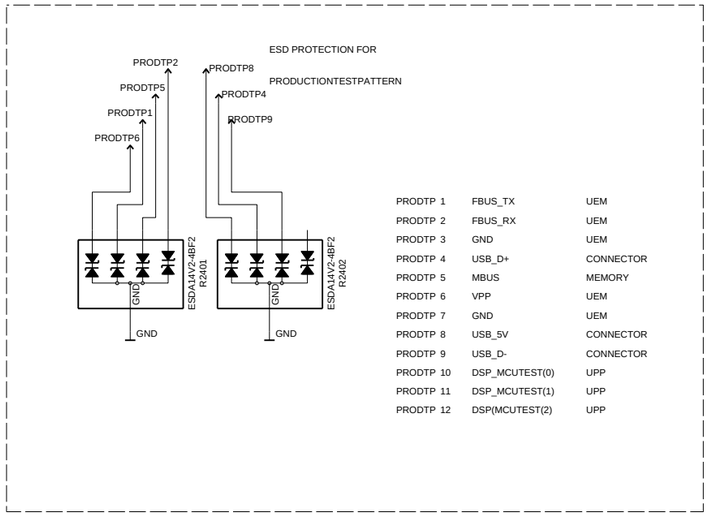
CMT UI v.0.0, ed.21

HEADINT(1:0)
G_KEY_UI(95:0)
SIMIF(3:0)
IHF_XEAR(1:0)
LCDUI(2:0)
AUDUEMCTRL(3:0)
KEYB(10:0)
EAR(1:0)
PUSL(3:0)
DIFCTRL(3:0)
GPIO(31:0)
DIFDATA(7:0)
SLOWAD(6:0)
MIC(2:0)

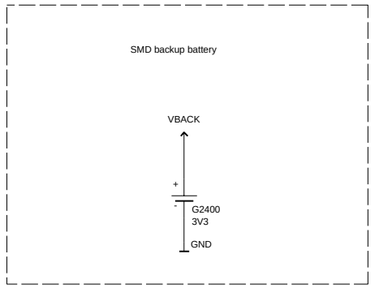








PRODTP 1	FBUS_TX	UEM
PRODTP 2	FBUS_RX	UEM
PRODTP 3	GND	UEM
PRODTP 4	USB_D+	CONNECTOR
PRODTP 5	MBUS	MEMORY
PRODTP 6	VPP	UEM
PRODTP 7	GND	UEM
PRODTP 8	USB_5V	CONNECTOR
PRODTP 9	USB_D-	CONNECTOR
PRODTP 10	DSP_MCUTEST(0)	UPP
PRODTP 11	DSP_MCUTEST(1)	UPP
PRODTP 12	DSP(MCUTEST(2)	UPP



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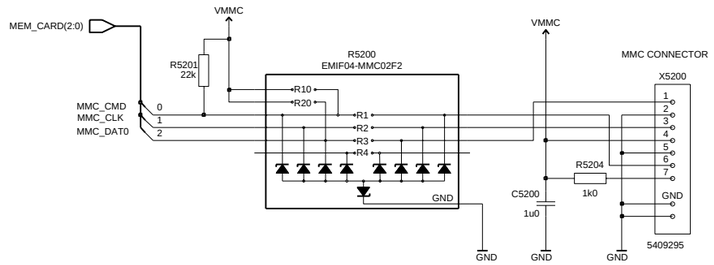
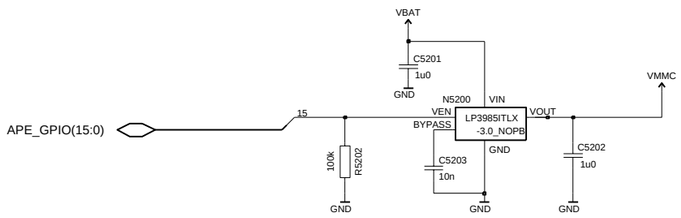
MMC v.0.0, ed.16





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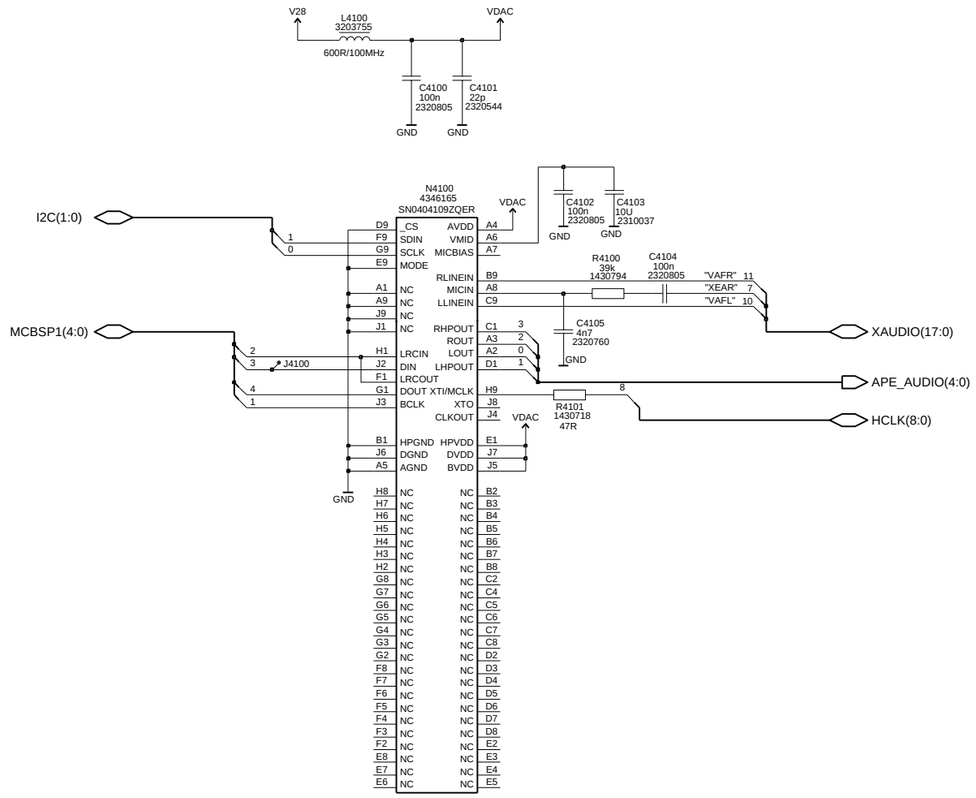
DAC Audio v.1.0, ed.141

APE_GPIO(15:0)
SLOWAD(6:0)
GENIO(31:0)
G_APE(15:0)



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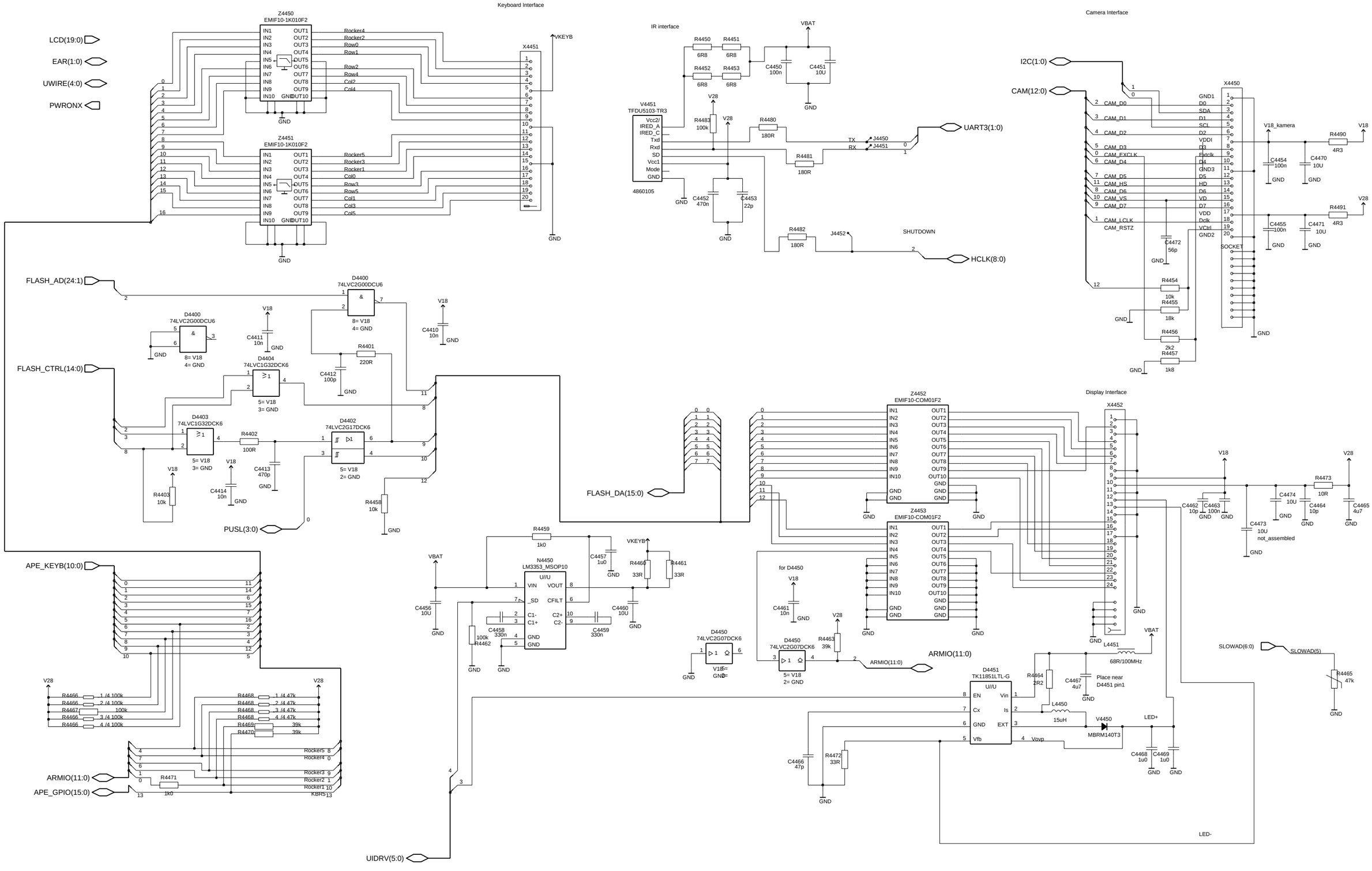
APE UI v.0.0, ed.84



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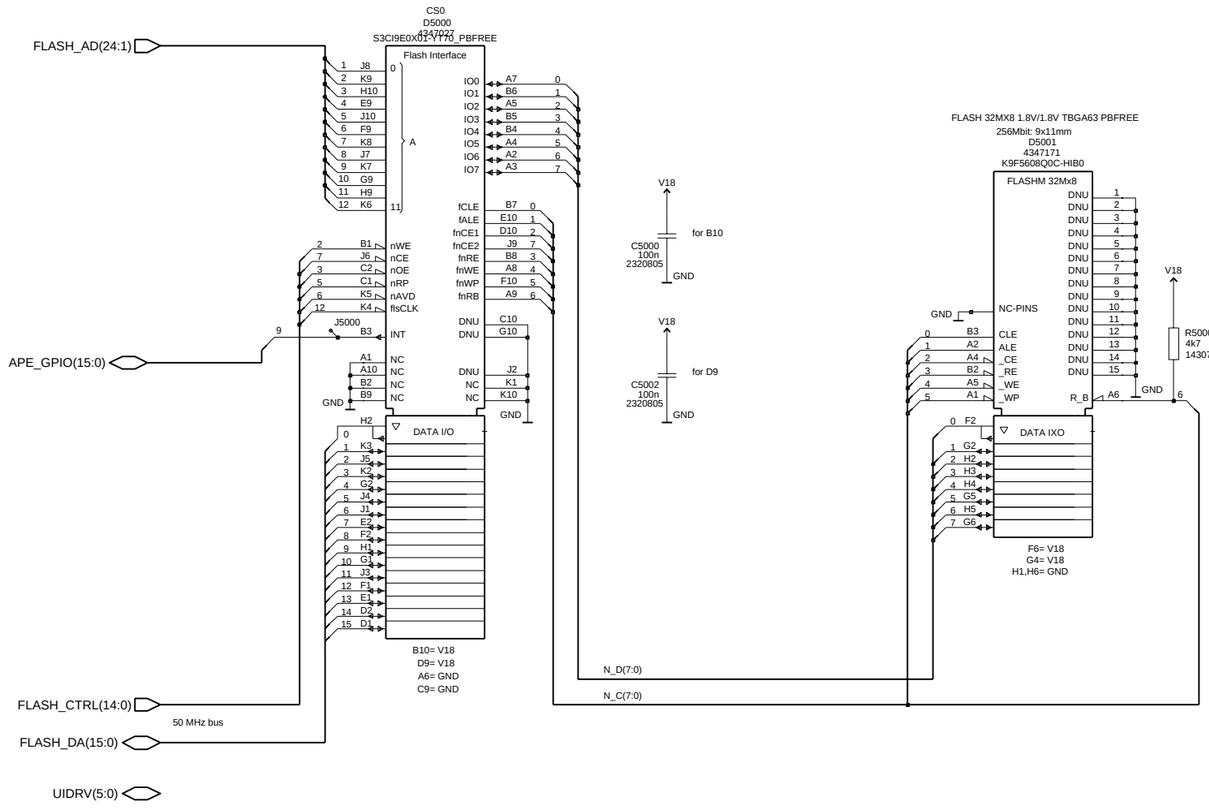
256Mbit NAND Flash and Seija Interface ASIC v.1.0, ed. 134



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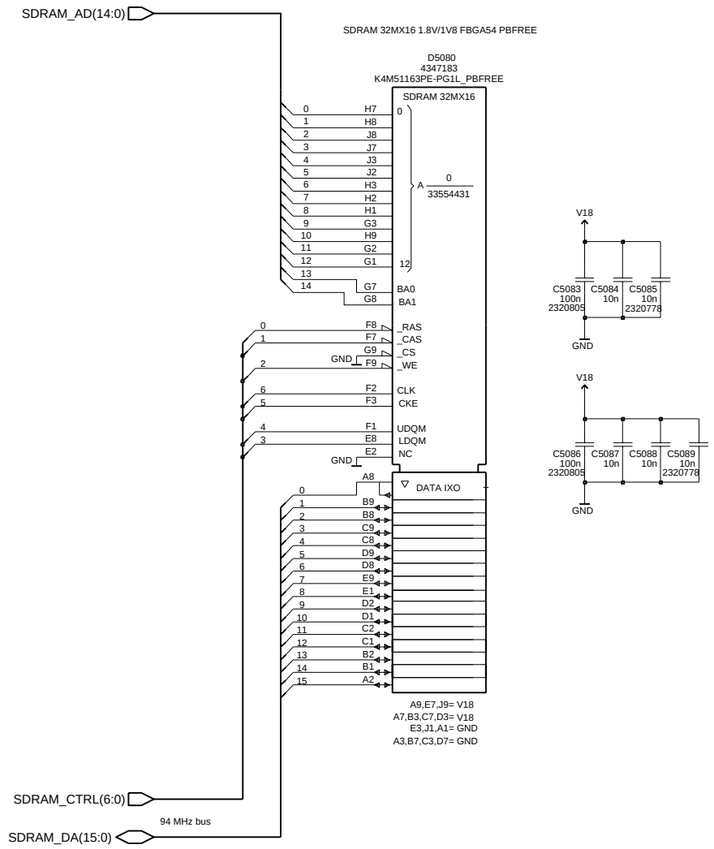
APE SDRAM 32Mx16 v.1.0, ed.28



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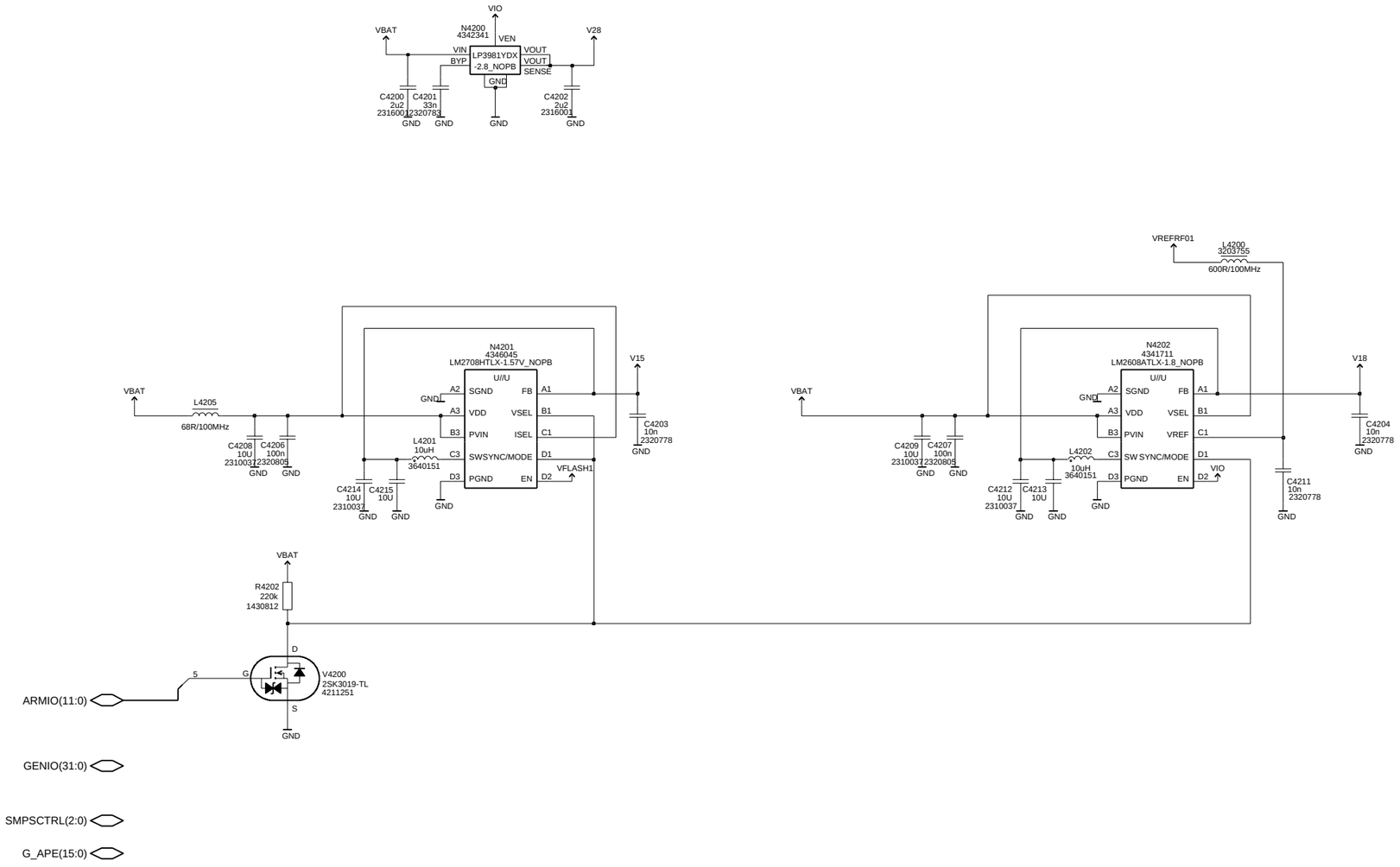
APE Power v.7.0, ed.113



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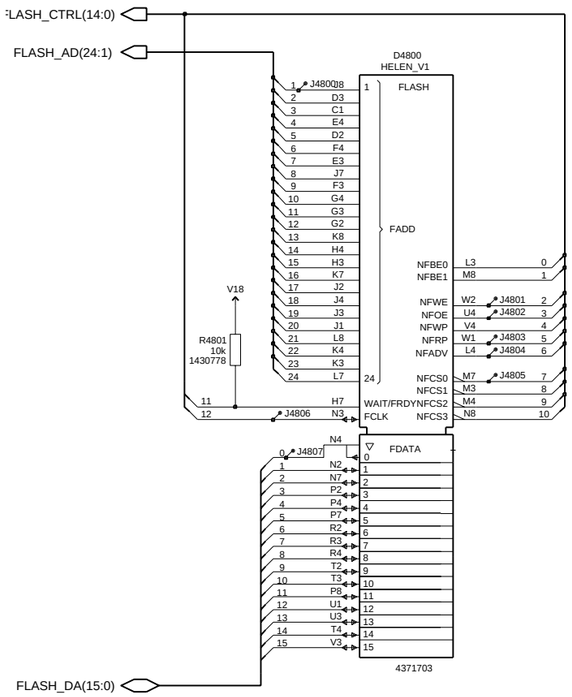
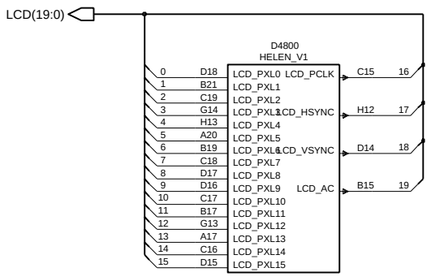
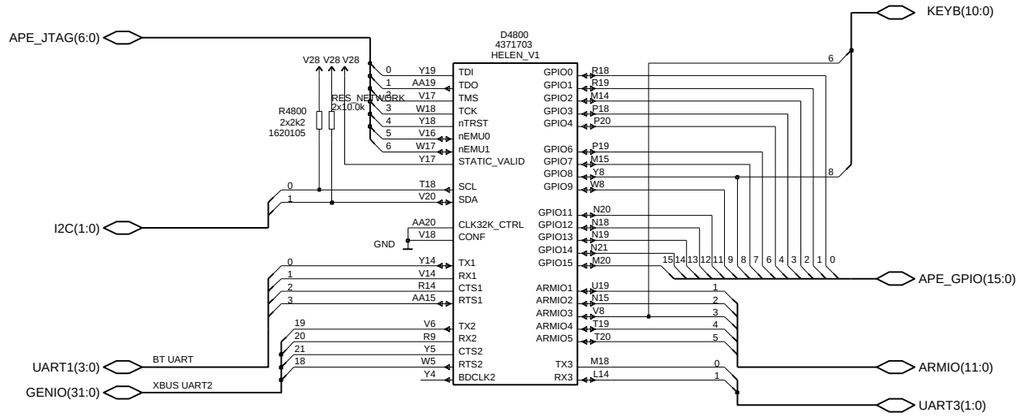
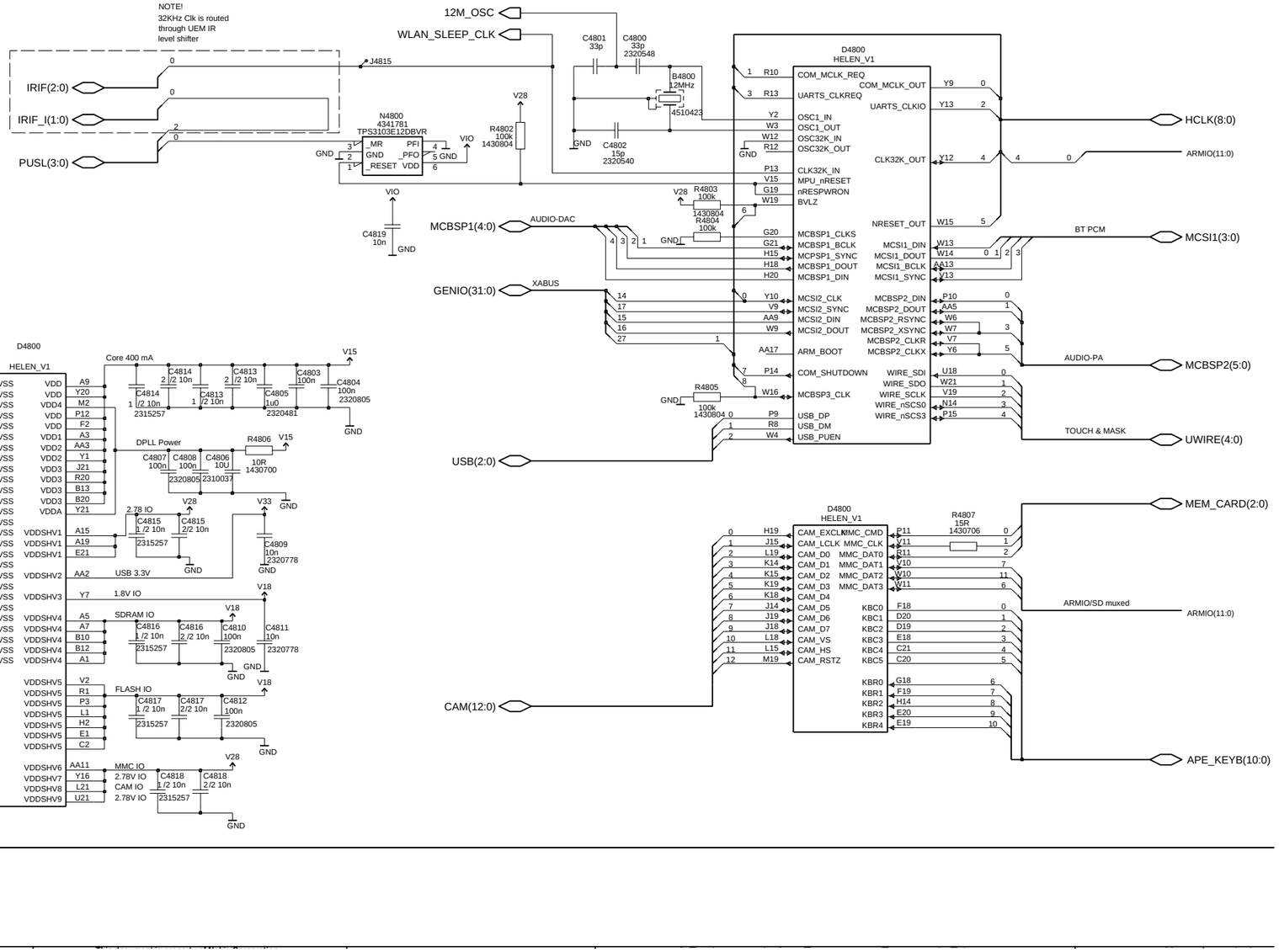
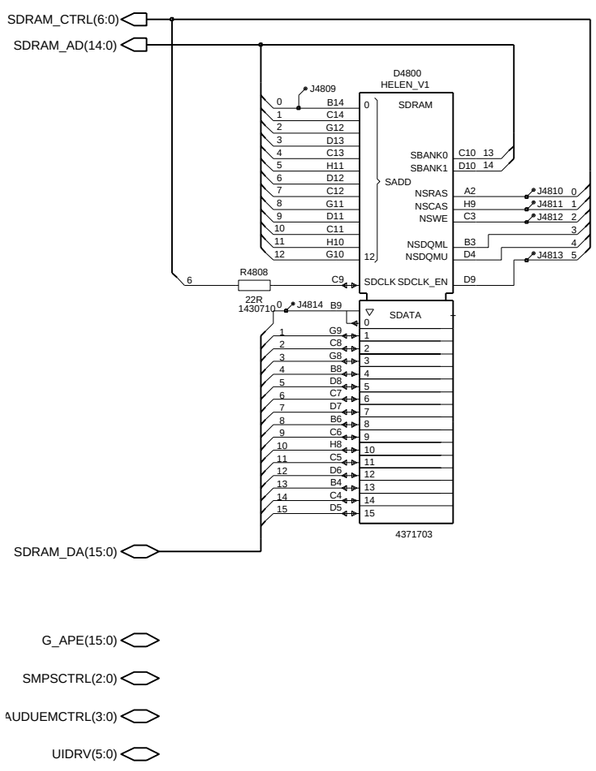
OMAP1510 v.7.0, ed.175



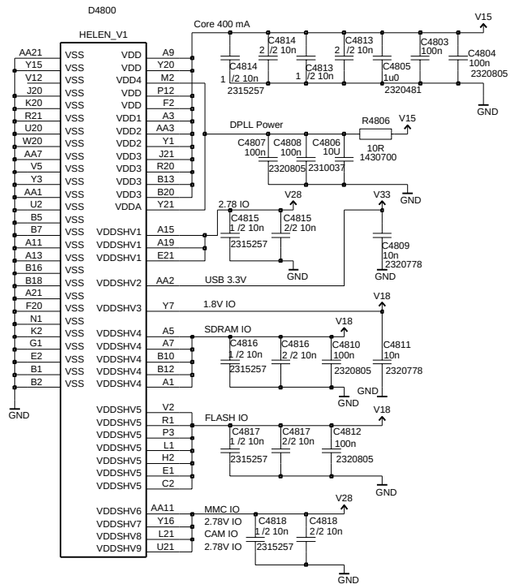








Do not connect V12 to GND!



G_APE(15:0)

SMPSCTRL(2:0)

AUDUEMCTRL(3:0)

UIDRV(5:0)

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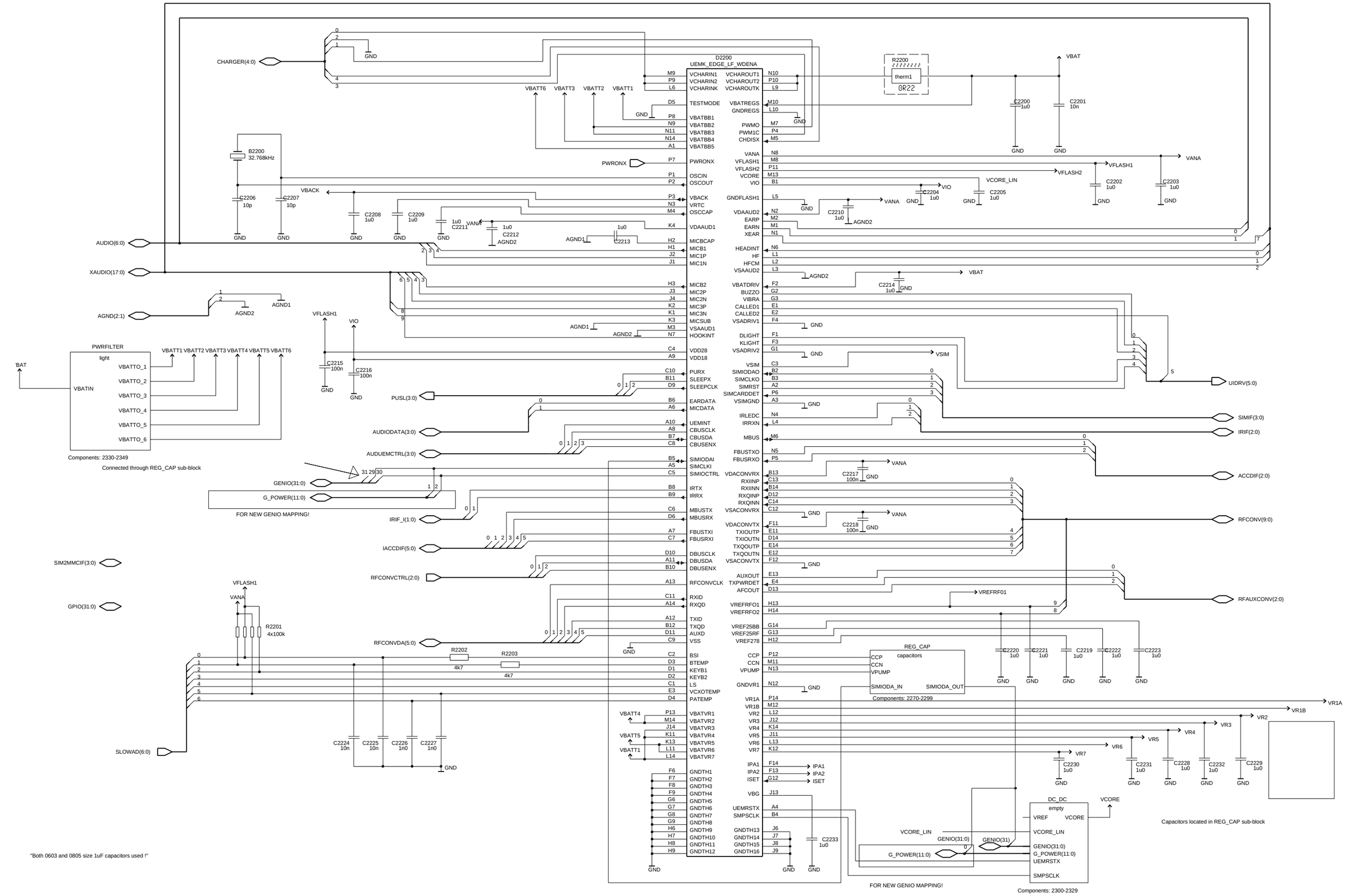
Discrete Power Management v.1.3, ed.128



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